L Number	Hits	Search Text	DB	Time stamp
1	388	257/785.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:06
8	1	(insulat$3 same land$1) and 257/785.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:13
15	140467	438/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:13
22	373	(insulat$3 same land$1) and 438/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:15
29	178	((insulat$3 same land$1) same (connect$3)) and ((insulat$3 same land$1) and 438/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:16
36	99	(compress$5 or pressur$6) and (((insulat$3 same land$1) same (connect$3)) and ((insulat$3 same land$1) and 438/$.ccls.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:18
43	73	257/$.ccls. and ((compress$5 or pressur$6) and (((insulat$3 same land$1) same (connect$3)) and ((insulat$3 same land$1) and 438/$.ccls.)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:41
50	0	(compress$4 same substrate$1 same (IC$1 or (integrate$1 adj circuit$5))) and (257/$.ccls. and ((compress$5 or pressur$6) and (((insulat$3 same land$1) same (connect$3)) and ((insulat$3 same land$1) and 438/$.ccls.))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:43
57	28	(substrate$1 same (IC$1 or (integrate$1 adj circuit$5))) and (257/$.ccls. and ((compress$5 or pressur$6) and (((insulat$3 same land$1) same (connect$3)) and ((insulat$3 same land$1) and 438/$.ccls.))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:53
64	2	6239496.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:55
71	2	6229209.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:55
-	157	substrate$1 same IC same (conductive near2 element$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
-	18	compress$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:04
-	3	crystal$1 same (compress$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 15:59

09/726,629

-	254523	257/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:00
-	66	257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
-	10	(compress$3 same (substrate$1 same IC same (conductive near2 element$1))) and (257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
-	17	(conductive near2 element$1) same compress$3 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
-	17	(conductive near2 element$1) same compress$4 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:23
-	4	(connector$1 or socket$1) same ((conductive near2 element$1) same compress$4 same crystal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:28
-	60	mount$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:29
-	13	(insulat$3) same (mount$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
-	498	257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
-	5	(substrate$1 same IC same (conductive near2 element$1)) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
-	6	(compress$4 same connect$4 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:12
-	8	(compress$4 same substrate$1 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:20
-	108	(compress$4 same substrate$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:21
-	16	(compress$4 same substrate$1 same (IC$1 or (integrate$1 adj circuit$5))) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:42

-	2	5821763.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:38
-	1715	bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:42
-	0	257/E23.078.ccls. and (bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:42
-	55	257/$.ccls. and (bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:05

US-PAT-NO: 6492718

DOCUMENT-IDENTIFIER: US 6492718 B2

TITLE: Stacked semiconductor device and semiconductor system

DATE-ISSUED: December 10, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ohmori; Jun	Yokkaichi	N/A	N/A	JP

US-CL-CURRENT: 257/686, 257/685 , 257/688 , 257/689 , 257/723 , 257/724 , 257/774 , **257/785** , 257/E25.023

ABSTRACT:

A stacked semiconductor device includes a plurality of stacked wiring substrates each having connection electrodes and wires connected to the connection electrodes and each mounted with a semiconductor device, a plurality of conductive via boards each interposed between adjacent two wiring substrates and having an opening for enclosing the semiconductor device, an uppermost wiring substrate formed on the top of the stacked wiring substrates and having wires connected to the connection electrodes, and a lowermost wiring substrate formed under the stacked wiring substrates and having wires connected to the connection electrodes, wherein heat radiation/shield conductive layers are formed on the uppermost and lowermost wiring substrates.

19 Claims, 19 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

---------- KWIC ---------

Detailed Description Text - DETX (7):

Each of the wiring substrates 1a-1d has a plurality of via-holes and connection electrodes 11 are buried in the via-holes of the **insulation** board or wiring substrate 1a-1d. Copper foils on the wiring substrate 1a-1d are patterned to form **lands** on the connection electrodes 11 and wires 12 on the substrates and electrically connected to the semiconductor device 5a-5d, respectively. The thickness of the semiconductor devices or chips 5a-5d is about 30 .mu.m to 200 .mu.m, preferably about 50 .mu.m to 150 .mu.m.

Detailed Description Text - DETX (9):

The conductive via **insulation** board 3a-3d are each formed of an **insulation** board, such as a poly-imide substrate and a printed circuit board each covered with copper foil wiring having a thickness of about 75 .mu.m. Connection electrodes 31 are buried in via-holes of the **insulation** board 3a-3d. A copper foil formed on each of the **insulation** boards 3a-3d is patterned to have **lands** as the connection electrodes 31 and wires (not shown) formed on the other area.

Current US Cross Reference Classification - CCXR (7):

257/785

US-PAT-NO: 6413798

DOCUMENT-IDENTIFIER: US 6413798 B1

TITLE: Package having very thin semiconductor chip, multichip module assembled by the package, and method for manufacturing the same

DATE-ISSUED: July 2, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Asada; Junichi	Kawasaki	N/A	N/A	JP

US-CL-CURRENT: 438/108, 257/E21.503 , 257/E23.124 , 257/E25.023 , 438/106 , 438/459

ABSTRACT:

A semiconductor package of this invention has an **insulating** substrates, wiring layers disposed on the surface of the **insulating** substrate, a semiconductor chip disposed in a device hole provided in the **insulating** substrate, inner-joint-conductors for **connecting** at least part of the bonding pads on the surface of the semiconductor chip to the corresponding inner-joint-conductors and **connection lands connected** to the wiring layers. The device hole is provided so that it goes through the center of the **insulating** substrate. The semiconductor chip is thinner than the **insulating** substrate. Then, this semiconductor chip is disposed in the device hole such that a bottom thereof is flush with a bottom plane of the **insulating** substrate. Further, this invention provides a MCM in which plural pieces of the thin semiconductor packages are laminated. In the MCM, the semiconductor packages are laminated such that top and bottom faces of the thin silicon chip are inverted. Predetermined **connection lands** are electrically **connected** to each other through a **connecting** conductor. This MCM has a high mechanical strength in its stacked structure and there is a low possibility that crack may occur in the package due to stress in the bending direction.

6 Claims, 26 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 15

---------- KWIC ---------

Abstract Text - ABTX (1):

A semiconductor package of this invention has an **insulating** substrates, wiring layers disposed on the surface of the **insulating** substrate, a semiconductor chip disposed in a device hole provided in the **insulating** substrate, inner-joint-conductors for **connecting** at least part of the bonding pads on the surface of the semiconductor chip to the corresponding inner-joint-conductors and **connection lands connected** to the wiring layers. The device hole is provided so that it goes through the center of the **insulating** substrate. The semiconductor chip is thinner than the **insulating** substrate. Then, this semiconductor chip is disposed in the device hole such that a bottom thereof is flush with a bottom plane of the **insulating** substrate.

Further, this invention provides a MCM in which plural pieces of the thin semiconductor packages are laminated. In the MCM, the semiconductor packages are laminated such that top and bottom faces of the thin silicon chip are inverted. Predetermined **connection lands** are electrically **connected** to each other through a **connecting** conductor. This MCM has a high mechanical strength in its stacked structure and there is a low possibility that crack may occur in the package due to stress in the bending direction.

Brief Summary Text - BSTX (12):

To achieve the above object, a first feature of the present invention inheres in a semiconductor package having: **insulating** substrates; wiring layers disposed on the surface of the **insulating** substrate; a semiconductor chip disposed in a device hole provided in the **insulating** substrate; inner-joint-conductors for **connecting** at least part of the bonding pads on the surface of the semiconductor chip to the corresponding wiring layers; and **connection lands connected** to the wiring layers. The device hole is provided so as to penetrate the central portion of the **insulating** substrate. The thickness of the semiconductor chip is smaller than that of the **insulating** substrate. Then, the semiconductor chip is disposed in the device hole such that a bottom thereof is flush with a bottom plane of the **insulating** substrate.

Brief Summary Text - BSTX (14):

A second feature of the present invention lies in laminated structure assembled by plural pieces of the semiconductor packages, each of the semiconductor packages is already stated in the first feature of the present invention. That is, according to the second feature of the present invention, first and second semiconductor packages, each having the above-described first feature of the present invention, are laminated, for example. The first semiconductor package has: a first **insulating** substrate; first wiring layers disposed on the first **insulating** substrate; a first semiconductor chip disposed in a first device hole of the first **insulating** substrate; first inner-joint-conductors for **connecting** the first bonding pads to the first internal wiring layers; first **connection lands connected** to the first wiring layers. On the other hand, the second semiconductor package has a second **insulating** substrate disposed above the first **insulating** substrate; second wiring layers disposed on the second **insulating** substrate; a second semiconductor chip disposed in the second device hole of the second **insulating** substrate; second inner-joint-conductors for **connecting** the second semiconductor chip to the second wiring layers; and second **connection lands** electrically **connected** to the first **connection lands**.

Brief Summary Text - BSTX (20):

A fourth feature of the present invention lies in a method for manufacturing a multi-chip module having the steps of: (a) thinning a first semiconductor chip having first bonding pads and a second semiconductor chip having second bonding pads to 10 .mu.m-150 .mu.m in thickness, respectively; (b) delineating package wirings on a main surface of a MCM substrate; (c) preparing a first **insulating** substrate having a first device hole and a second **insulating** substrate having a second device hole; (d) delineating first wiring layers and first **connection lands connected** to the first wiring layers on the first **insulating** substrate; (e) delineating second wiring layers and second **connection lands connected** to the second wiring layers on the second **insulating** substrate; (f) placing the first and second **insulating** substrates on a table so as to mount the first and second semiconductor chips in the first and second device holes; (g) **connecting** the first bonding pads to the corresponding first wiring layers through first inner-joint-conductors; (h) **connecting** the second bonding pads to the corresponding second wiring layers through second inner-joint-conductors; (i) sealing the first semiconductor chip and the first inner-joint-conductor with resin and sealing the second semiconductor chip and

the second inner-joint-conductor with resin; j) mounting the first **insulating** substrate on the MCM substrate so as to electrically **connect** the package wirings to the first **connection lands**; and (k) mounting the second **insulating** substrate on the first **insulating** substrate so as to electrically **connect** the first **connection lands** to the second **connection lands**.

Detailed Description Text - DETX (7):

As shown in FIG. 3A, the semiconductor package according to the first embodiment of the present invention has an **insulating** substrate 111, wiring layers 121a, . . . , 121j, . . . disposed on the surface of this **insulating** substrate 111, a semiconductor chip 131 disposed in the device hole 731 provided in the **insulating** substrate 111. A plurality of bonding pads 821a, . . . , 821j, . . . are disposed on the surface of the semiconductor chip 131. The semiconductor package according to the first embodiment further has inner-joint-conductors (inner leads) 721a, . . . , 721j, . . . for **connecting** the bonding pads 821a, . . . , 821j, . . . to the corresponding wiring layers 121a, . . . , 121j, ... And **connection lands** 151a, . . . , 151j, . . . are **connected** to the wiring layers 121a, . . . , 121j . . . . The device holes 731 are provided so as to penetrate a central portion of the **insulating** substrate 111. The semiconductor chip 131 is made thinner than the **insulating** substrate 111. The semiconductor chip 131 is disposed in the device hole 731 such that its bottom surface is exposed so that the bottom level is flush with the bottom plane of the **insulating** substrate 111. The **insulating** substrate 111 is an **insulating** polymer film having a thickness of, for example, 75 .mu.m. As the **insulating** polymer film, for example, polyimide film such as tape automated bonding (TAB) tape is preferable. The **insulating** substrate (**insulating** polymer film) 111 acts as "an interposer" of the MCM shown in FIG. 3B.

Detailed Description Text - DETX (9):

Each side of the rectangular silicon chip 131 is smaller than sides of rectangular window serving as the device hole 731. The thickness of the silicon chip 131 is elected to be, for example, 50 .mu.m. This silicon chip 131 is buried in the device hole 731 in a face up orientation. The respective bonding pads 821a, . . . , 821j, . . . provided on perimeter of the surface of the silicon chip 131 are bonded to the inner leads 721a, . . . , 721j, . . . through a thermocompression process called "gang bonding". This process is referred as "inner lead bonding (ILB)". The inner leads 721a, . . . , 721j, . . . can be bonded to bonding pads 821a, . . . , 821j, . . . using soldering, by heating with **pressure**. As the interposer 111, another flexible substrate different from the TAB tape can be employed. Further, instead of the flexible substrate a rigid substrate, or a polymer substrate reinforced with woven fibers (e-glass, s-glass, quartz, aramid etc.) may be used as the interposer 111. As the rigid substrate, a very common laminate material, consisting of epoxy and e-glass may be used. This glass epoxy is referred as "American National Standard Institute (ANSI) FR-4 grade substrate".

Detailed Description Text - DETX (11):

A sealed resin layer 141 is formed so as to cover a area in which the silicon chip 131 is buried in the device hole 731 and an adjacent area in which the **connecting** portions between the bonding pads 821a, . . . , 821j, . . . and inner leads 721a, . . . , 721j, . . . are included. This sealed resin layer 141 is buried in a gap between the sidewall of the device hole 731 and the semiconductor chip 131. The sealed resin layer 141 is buried so as to have the same bottom level as the bottom plane of the **insulating** substrate 111 as shown in FIG. 3A. The **connection lands** 151a, . . . , 151j, . . . are **connected** to the Cu wiring layers 121a, . . . , 121j, . . . Through holes 741a, . . . , 741j . . . , . . . are respectively formed just below the **connection lands** 151a, . . . , 151j, . . . within the **insulating** substrate 11. The thickness of the thin semiconductor package according to the first embodiment of the present invention as shown in FIG. 3A can be reduced to, for

example, less than 200 .mu.m.

Detailed Description Text - DETX (13):
The first semiconductor package has a first **insulating** substrate 111, first wiring layers 121a, . . . , 121j, . . . disposed on the surface of the first **insulating** substrate 111, a first semiconductor chip 131 disposed in the first device hole of the first **insulating** substrate 111, first inner-joint-conductors (inner leads) 721a, . . . , 721j, . . . for **connecting** at least part of the first bonding pads 821a, . . . , 821j, . . . on the surface of the first semiconductor chip 131 to at least part of the corresponding first wiring layers 121a, . . . , 121j . . . . First **connection lands** 151a, . . . , 151j, . . . are **connected** to the first wiring layers 121a, . . . 121j, ... The first device hole is formed so as to penetrate the central portion of the first **insulating** substrate 111. The first semiconductor chip 131 is disposed in the first device hole such that its bottom surface is exposed so as to be flush with the bottom plane of the first **insulating** substrate 111. First through holes are formed just below the first **connection lands** 151a, . . . , 151j , . . . within the first **insulating** substrate 111. First stud conductors 251a, . . . , 251j, . . . are buried in the first through holes so as to be **connected** to the package wirings 17a, . . . , 17j, . . . on the surface of the MCM substrate 16. A first sealing resin 141 is buried in a gap between the sidewall of the first device hole and the first semiconductor chip 131. The bottom surface of the first sealing resin 141 is configured such that it flushes with the bottom plane of the first **insulating** substrate 111.

Detailed Description Text - DETX (14):
On the other hand, the second semiconductor package has a second **insulating** substrate 112 disposed above the first **insulating** substrate 111, second wiring layers 122a, . . . , 122j, . . . disposed on the surface of the second **insulating** substrate 112, second semiconductor chip 132 disposed in the second device hole of the second **insulating** substrate 112, second inner-joint-conductors (inner leads) 722a, . . . , 722j, . . . for **connecting** at least part of the second bonding pads 822a, 822j on the surface of the second semiconductor chip 132 to at least part of the corresponding second wiring layers 122a, . . . , 122j, . . . and second **connection lands** 152a, . . . , 152j, . . . **connected** to the second wiring layers 122a, . . . , 122j, . . . and electrically **connected** to the first **connection lands** 151a, . . . , 151j, ... The first **connection lands** 151a, . . . 151j, . . . and the second **connection lands** 152a, . . . , 152j, . . . are **connected** to each other through **land** joint conductors 252a, . . . , 252j . . . . As the **land** joint conductors 252a, . . . , 252j, . . . , solder or other conductive adhesive may be used. The second device hole is formed so as to penetrate the central portion of the second **insulating** substrate 112. The second semiconductor chip 132 is disposed in the second device hole such that its bottom is flush with the bottom plane of the second **insulating** substrate 112. The second through hole is formed in the second **insulating** substrate just above each of the second **connection lands** 152a, . . . , 152j, ... The second sealed resin 142 is buried in a gap between the sidewall of the second device hole and the second semiconductor chip 132. The bottom of the second sealed resin 142 is exposed so that it is flush with the bottom plane of the second **insulating** substrate 112. Second stud conductors 253a, . . . , 253j, . . . are buried in the second through holes.

Detailed Description Text - DETX (15):
The third semiconductor package has a third **insulating** substrate 113, third wiring layers 123a, . . . , 123j, . . . disposed on the surface of the third **insulating** substrate 113, third semiconductor chip 133 disposed in the third device hole of the third **insulating** substrate 113, third inner-joint-conductors (inner leads) 723a, . . . , 723j, . . . for **connecting** at least part of the

third bonding pads 823a, . . . , 823j, . . . on the surface of the third semiconductor chip 133 to at least part of the corresponding third wiring layers 123a, . . . , 123j, ... And third **connection lands are connected** to the third wiring layers 123a, . . . , 123j, ... Further, the third semiconductor package has third through holes formed just below the third **connection lands** 153a, . . . , 153j, . . . in the third **insulating** substrate 113. The second stud conductors 253a, . . . , 253j, . . . extends from a side of the second semiconductor package so as to be buried in each of the third through holes. The third device hole is formed so as to penetrate the central portion of the third **insulating** substrate 113. The third semiconductor chip 133 is disposed in the third device hole such that its bottom is exposed. The bottom of the third semiconductor chip 133 is configured such that it is flush with the bottom plane of the third **insulating** substrate 113.

Detailed Description Text - DETX (19):

As shown in FIG. 3B, the **insulating** substrates 112, 113 are stacked so that their back sides face each other. Then, the through holes just above the **connection lands** 152a, . . . , 152j, . . . of the second level become continuous with the through holes just below the **connection lands** 153a, . . . , 153j, . . . of the third level. If a hole is made in the center of each of the respective **lands** 151a, 152a, 153a, 154a, . . . , 151j, 152j, 153j, 153j, . . . continuous through holes are produced from the **lands** 154a, . . . , 154j, . . . of the fourth level up to the package wirings 17a, . . . , 17j, . . . running on the surface of the MCM substrate 16. With this condition, the through holes are filled with conductive adhesive and then, the conductive adhesive is left to harden, thereby the **connection lands** 151a, 152a, 153a, 154a, 151j, 152j, 153j, 15j being electrically **connected** to the package wirings 17a, . . . , 17j, . . . of the MCM substrate 116. Then, the MCM according to the first embodiment has been achieved.

Detailed Description Text - DETX (28):

(d) Then, as shown in FIG. 6D, the flat ring 25 to which the divided individual silicon chips 131, 132, 133, 134, . . . are bonded and fixed is installed on a die bonding unit. Then, a downward **pressure** is applied to the pattern forming face 41 through the surface protecting tape 26 using a tool 30 such as a pick-up needle. Consequently, the silicon chips 131, 132, 133, 134, . . . are separated from the surface protecting tape 26. In this manner, the silicon chips 131, 132, 133, 134, . . . each having a thickness of for example 50 .mu.m are completed.

Detailed Description Text - DETX (29):

(e) Next, an **insulating** polymer film (for example, polyimide film) tape, which is 75 .mu.m thick, having periodically arranged device holes 731, 731, 731, . . . in the center thereof is prepared. Copper (Cu) foil 18 .mu.m thick is laminated entirely on the surface of the **insulating** substrate (**insulating** polymer film) 111 in the form of tape. Then a interposer 111 in which Cu wiring layers 121a, . . . , 121j, . . . are formed as shown in FIG. 6E by selective etching with photolithography or the like, are prepared. Although not shown, each of the first **connection lands** 151a, . . . , 151j, . . . merges the corresponding Cu wiring layers 121a, . . . , 121j, . . . so as to form an integral Cu wiring pattern. End portions of the Cu wiring layers 121a, . . . , 121j, . . . constituting the inner leads 721a, . . . , 721j, . . . are protruded from both sides into inside of the device holes 731, 731, 731, . . . periodically arranged on the interposer 111. Then, the end portions of the inner leads 721a, . . . , 721j, . . . are plated with Au films to facilitate **connection** thereof to the bonding pads 821a, . . . , 821j . . . . Meanwhile, it is assumed that the thickness of the **insulating** substrate (**insulating** polymer film) 111 is for example, 75 .mu.m and that the thickness of the Cu wiring layers 121a, . . . , 121j, . . . is 18 .mu.m.

Detailed Description Text - DETX (46):
The Cu wiring layers 611a, . . . , 611j, . . . of the first **insulating** substrate (first interposer) 601 are stretching out from the surface of the thin silicon chip 131 so that the first **connection** lands,621a, . . . , 621j, . . . are formed. Likewise, the Cu wiring layers 612a, . . . , 612j, . . . of the second **insulating** substrate (second interposer) 602 are stretching out from the surface of the thin silicon chip 132 so that the second **connection lands** 622a, . . . , 622j, . . . are formed. Further, the Cu wiring layers 613a, . . . , 613j, . . . of the third **insulating** substrate (third interposer) 603 are stretching out from the surface of the thin silicon chip 133 so that the third **connection lands** 623a, . . . , 623j, . . . are formed. Further, the Cu wiring layers 614a, . . . , 614j, . . . of the fourth **insulating** substrate (fourth interposer) 604 are stretching out from the surface of the thin silicon chip 134 so that the fourth **connection lands** 624a, . . . , 624j, . . . are formed. The first **connection lands** 621a, . . . , 621j, . . . are **connected** to the package wirings 17a, . . . , 17j, . . . through first outer-joint-conductors 651a, . . . , 651j, . . . such as solder ball. The second **connection lands** 622a, . . . , 622j, . . . are **connected** to the first **connection lands** 621a, . . . , 621j, . . . through the second outer-joint-conductors 652a, . . . , 652j . . . . The third **connection lands** 623a, . . . , 623j, . . . are **connected** to the second **connection lands** 622a, . . . , 622j, . . . through the third outer-joint-conductors 653a, . . . , 653j . . . . The fourth **connection lands** 624a, . . . , 624j, . . . are **connected** to the third **connection lands** 623a, . . . , 623j, . . . through the fourth outer-joint-conductors 654a, . . . , 654j . . . .

Claims Text - CLTX (5):
(d) delineating first wiring layers and first **connection lands connected** to said first wiring layers on a surface of said first **insulating** substrate;

Claims Text - CLTX (6):
(e) delineating second wiring layers and second **connection lands connected** to said second wiring layers on a surface of said second **insulating** substrate;

Claims Text - CLTX (11):
(j) mounting said first **insulating** substrate on said MCM substrate so as to electrically **connect** said package wirings to said first **connection lands**; and

Claims Text - CLTX (12):
(k) mounting said second **insulating** substrate on said first **insulating** substrate so as to electrically **connect** said first **connection lands** to said second **connection lands**.

Current US Original Classification - CCOR (1):
438/108

Current US Cross Reference Classification - CCXR (1):
257/E21.503

Current US Cross Reference Classification - CCXR (2):
257/E23.124

Current US Cross Reference Classification - CCXR (3):

257/E25.023

Current US Cross Reference Classification - CCXR (4):
438/106

Current US Cross Reference Classification - CCXR (5):
438/459

US-PAT-NO: 6372549

DOCUMENT-IDENTIFIER: US 6372549 B1

TITLE: Semiconductor package and semiconductor package fabrication method

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Urushima; Michitaka	Tokyo	N/A	N/A	JP

US-CL-CURRENT: 438/118, 257/678 , 257/684 , 257/701 , 257/E21.503 , 257/E23.067 , 257/E23.069 , 438/106 , 438/107 , 438/108

ABSTRACT:

The semiconductor package is highly reliable and has a construction that enables an improvement of fabrication yield and that can greatly reduce the number of steps and the amount of time required for those steps. The semiconductor package has a construction in which wiring layer 14 is supported by insulating film 13 over a range corresponding to chip electrodes 12 of semiconductor chip 11. In the fabrication of this semiconductor package, the semiconductor chip 11 is mounted on an interposer constituted by the wiring layer 14, insulating film 13, and adhesive layer 16 by inserting bumps 17 into holes 16a in adhesive layer 16, following which the metal junctions between wiring layer 14 and all bumps 17 as well as adhesion between semiconductor ship 11 and wiring tape 4 by means of adhesive layer 16 are realized simultaneously by using a heater plate to apply heat to adhesive layer 16 and inner lead connectors while pressing wiring tape 4 across substantially the entire range of the chip electrode formation surface.

11 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Brief Summary Text - BSTX (7):

a semiconductor package in which an interposer, in which a wiring layer of, for example, copper wiring having a prescribed wiring pattern is arranged on an **insulating** base material such as polyimide tape, is adhered to the electrode formation surface of a semiconductor chip by way of an adhesive layer; electrodes, such as aluminum electrodes, of the semiconductor chip are electrically **connected** to a wiring layer by way of bumps such as gold ball bumps; i.e., by the so-called flip-chip method; and external **connectors** are provided on the side of the wiring layer that is opposite from the junction surface with the semiconductor chip. In this case, external **connectors** are, for example, solder balls that are attached to **lands** of the wiring layer or similar **lands**.

Brief Summary Text - BSTX (14):

When assembling semiconductor package 2, the adhesive surface that is formed

by adhesive layer 26 of wiring tape 5 is temporarily secured on the electrode formation surface of semiconductor chip 21 on which chip electrodes 22 are formed; bonding tool 50 is passed through holes 29a and placed in contact with copper wiring 24, and **pressure** and ultrasonic waves are applied to the connector portion (inner lead connectors) chip electrode 22 and filled copper bumps 27. In a case in which semiconductor chip 21 is provided with, for example, 1000 chip electrodes 22, this bonding operation by means of bonding tool 50 must be carried out a total of 1000 times.

Brief Summary Text - BSTX (15):
Next, complete adhesion between semiconductor chip 21 and wiring tape 5 can be obtained by applying appropriate heat and **pressure** to adhesive layer 26.

Brief Summary Text - BSTX (19):
When assembling semiconductor package 3, the adhesive surface that is arranged on adhesive layer 36 of wiring tape 6 is temporarily secured to the electrode formation surface of semiconductor chip 31 upon which gold ball bumps 37 are arranged at chip electrodes 32, i.e., temporarily secured on the surface on which chip electrodes 32 are formed; and bonding tool 50 is passed through holes 33a and placed against copper wiring 34, following which **pressure** and ultrasonic waves are applied to the connectors (inner lead connectors); i.e., between gold ball bumps 37 and chip electrodes 32 and between gold ball bumps 37 and copper wiring 34. In a case in which, for example, 1000 chip electrodes 32 are provided on semiconductor chip 31, this bonding operation by bonding tool 50 must be performed a total of 1000 times.

Brief Summary Text - BSTX (20):
An appropriate degree of heat and **pressure** are then applied to adhesive layer 36 to obtain complete adhesion between semiconductor chip 31 and wiring tape 6.

Brief Summary Text - BSTX (21):
In the publications of Japanese Patent Laid-open No. 321157/95 and Japanese Patent Laid-open No. 102474/96, bonding is achieved when assembling the semiconductor package by first carrying out single-point bonding, which is the bonding operation by means of bonding tool 50, and then applying **pressure** and heat.

Brief Summary Text - BSTX (26):
Furthermore, both examples of the prior art employ the application of ultrasonic waves and **pressure** by a bonding tool for each chip electrode (single-point bonding) to realize connection in the process of bonding the electrodes of the semiconductor chip and the wiring layer through the use of bumps according to the flip-chip method. There is consequently the problem that the more pins used by a semiconductor chip, the more time and labor that are required, and the higher the fabrication cost.

Brief Summary Text - BSTX (51):
In the method of fabricating a semiconductor package, the **pressure** of the level surface of a heated **pressure** part against the rear surface of the semiconductor chip may be used to heat the inner lead connectors that include the adhesive layer and bumps while pressing the interposer against substantially the entire surface of the electrode formation surface of the semiconductor chip.

Brief Summary Text - BSTX (53):
The method of fabricating a semiconductor package may be realized by

mounting a plurality of semiconductor chips on a uniform interposer, arranging this interposer on a silicon sheet, and then applying heat and **pressure** by a heater plate from above the semiconductor chips within a vacuum.

Brief Summary Text - BSTX (54):
In the method of fabricating a semiconductor package, the conditions for applying heat and **pressure** to cause adhesion and the conditions for applying heat and **pressure** for obtaining the metal junction may be set substantially equal.

Brief Summary Text - BSTX (55):
This method enables the application of heat and **pressure** that is neither insufficient nor excessive to both the adhesive layer and the inner lead connectors. This has the advantages of enabling satisfactory states of both adhesion and metal junction and enabling a further shortening of the time required for fabrication steps.

Detailed Description Text - DETX (25):
At this time, copper wiring 14 is supported by insulating film 13 within the range that corresponds to chip electrodes 12, and the **pressure** of the heater plate can therefore be reliably transmitted to the inner lead connectors. In addition, a portion of the silicon sheet is forced into holes 13a and supports copper wiring 14, whereby wiring tape 4 is adequately pressed against the surface of semiconductor chip 11 on which chip electrodes 12 are formed even within the range of holes 13a.

Detailed Description Text - DETX (26):
Excellent adhesion without the occurrence of entrapped air between semiconductor chip 1 and adhesive layer 16 can be achieved because this **pressure** is exerted in a vacuum.

Detailed Description Text - DETX (27):
The adhesive that is used on adhesive layer 16 is selected in advance such that the heating value and **pressure** value for obtaining optimum adhesion are substantially equal to the heating value and **pressure** value for obtaining optimum metal junctions.

Detailed Description Text - DETX (42):
In the step for simultaneously realizing inner lead bonding and adhesion, the heating temperature of the heater plate was 300.degree. C., the **pressure** value was 980 mN per bump, and the pressing time was 20 seconds per frame. An excellent adhesion state and metal junction state were achieved under these conditions.

Detailed Description Text - DETX (43):
In the present invention as described hereinabove, the wiring layer is supported by the insulating substrate within the range that corresponds to the electrodes of the semiconductor chip, and a tool such as a heater plate is pressed against the rear surface of the semiconductor chip, whereby heat can be applied to the adhesive layer and inner lead connectors while applying **pressure** against the interposer over substantially the entire surface of the electrode formation surface of the semiconductor chip. As a result, the present invention simultaneously realizes the inner lead bonding of all electrodes on the semiconductor chip and the sealing of the adhesive and junction surfaces between the semiconductor chip and the interposer. The present invention therefore has the effect of greatly reducing the number of steps in semiconductor package fabrication and greatly reducing the amount of time

required in steps, and is extremely advantageous when dealing with a large number of pins.

Claims Text - CLTX (9):
2. A method of fabricating a semiconductor package according to claim 1 wherein metal junctions between said wiring layer and said bumps and adhesion between said semiconductor chip and said interposer by means of said adhesive layer are realized by the **pressure** of a level surface of a heated **pressure** part against the rear surface of said semiconductor chip to apply heat to inner lead connectors that include said adhesive layer and said bumps while pressing said interposer against substantially the entire surface of the electrode formation surface of said semiconductor chip.

Claims Text - CLTX (10):
3. A method of fabricating a semiconductor package according to claim 2 wherein the heat and **pressure** conditions for obtaining said adhesion are set substantially equal to the heat and **pressure** conditions for obtaining said metal junctions.

Claims Text - CLTX (13):
6. A method of fabricating a semiconductor package according to claim 5 wherein metal junctions between said wiring layer and said bumps and adhesion between said semiconductor chip and said interposer by means of said adhesive layer are realized by pressing a level surface of a heated **pressure** part against the rear surface of said semiconductor chip to heat inner lead connectors that include said adhesive layer and said bumps while pressing said interposer against substantially the entire surface of the electrode formation surface of said semiconductor chip.

Claims Text - CLTX (14):
7. A method of fabricating a semiconductor package according to claim 6 wherein the heat and **pressure** conditions for obtaining said adhesion are set substantially equal to the heat and **pressure** conditions for obtaining said metal junctions.

Claims Text - CLTX (16):
9. A method of fabricating a semiconductor package according to claim 5 wherein a plurality of said semiconductor chips are mounted on a uniform said interposer, this interposer is arranged on a silicon sheet, and heat and **pressure** are applied by a heater plate from above said semiconductor chips in a vacuum.

Claims Text - CLTX (17):
10. A method of fabricating a semiconductor package according to claim 9 wherein the heat and **pressure** conditions for obtaining said adhesion are set substantially equal to the heat and **pressure** conditions for obtaining said metal junctions.

Current US Original Classification - CCOR (1):
438/118

Current US Cross Reference Classification - CCXR (1):
257/678

Current US Cross Reference Classification - CCXR (2):

257/684

Current US Cross Reference Classification - CCXR (3):
257/701

Current US Cross Reference Classification - CCXR (4):
257/E21.503

Current US Cross Reference Classification - CCXR (5):
257/E23.067

Current US Cross Reference Classification - CCXR (6):
257/E23.069

Current US Cross Reference Classification - CCXR (7):
438/106

Current US Cross Reference Classification - CCXR (8):
438/107

Current US Cross Reference Classification - CCXR (9):
438/108

US-PAT-NO: 6372547

DOCUMENT-IDENTIFIER: US 6372547 B1

TITLE: Method for manufacturing electronic device with resin layer between chip carrier and circuit wiring board

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamura; Yoshifumi	Osaka	N/A	N/A	JP
Bessho; Yoshihiro	Osaka	N/A	N/A	JP
Itagaki; Minehiro	Osaka	N/A	N/A	JP

US-CL-CURRENT: 438/118, 257/E21.511 , 257/E23.067 , 257/E23.069 , 438/126 , 438/127

ABSTRACT:

In BGA (Ball Grid Array), LGA (Land Grid Array) and the like, a resin layer is formed between an external connecting electrode of a chip carrier and a circuit wiring board. Consequently, the external connecting electrode can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external connecting electrode and the circuit wiring board. Thus, the reliability in a thermal shock test can be enhanced. A connecting wiring which is conducted to an electrode of a semiconductor device is provided on a surface of an electrical insulating board, and the external connecting electrode for connection to a connecting electrode of the circuit wiring board is provided on a back face of the electrical insulating board. The external connecting electrode has a solder ball made of a conductor, and the resin layer formed on the side portion thereof.

8 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Abstract Text - ABTX (1):

In BGA (Ball Grid Array), LGA (Land Grid Array) and the like, a resin layer is formed between an external connecting electrode of a chip carrier and a circuit wiring board. Consequently, the external connecting electrode can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external connecting electrode and the circuit wiring board. Thus, the reliability in a thermal shock test can be enhanced. A connecting wiring which is conducted to an electrode of a semiconductor device is provided on a surface of an electrical insulating board, and the external connecting electrode for connection to a connecting electrode of the circuit wiring board is provided on a back face of the electrical insulating board. The external connecting electrode has a solder ball made of a conductor, and the resin layer formed on the side portion thereof.

Detailed Description Text - DETX (46):

Then, a hole having a diameter of 0.5 mm is formed on a sheet made of a thermoplastic polyoxyether resin which has a thickness of 0.15 mm by means of a punching machine. The softening point of the resin sheet is 160.degree. C. The external electrode of the chip carrier and the hole portion of the sheet are aligned so as to correspond to each other. The sheet may be temporarily bonded to the chip carrier in the following manner. More specifically, a flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon) is heated to about 160.degree. C. The aligned chip carrier is temporarily bonded to the sheet by means of the heated stainless steel tray. Thus, the sheet can be temporarily bonded to the chip carrier. In addition, the following method can be performed. More specifically, the aligned chip carrier is heated to about 160.degree. C. on the hot plate, and **pressurized** for a desired time by the flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon). Thus, the sheet made of a resin can be bonded to the chip carrier. While the polyoxyether resin has been used for the sheet in the present example, a resin having a softening point in the range of 160.degree. C. up to a solder paste melting temperature or less also has the same effects. The resin layer should have a softening point of 160.degree. C. or more so as not to be softened by a shelf test at a temperature of 150.degree. C.

Current US Original Classification - CCOR (1):

438/118

Current US Cross Reference Classification - CCXR (1):

257/E21.511

Current US Cross Reference Classification - CCXR (2):

257/E23.067

Current US Cross Reference Classification - CCXR (3):

257/E23.069

Current US Cross Reference Classification - CCXR (4):

438/126

Current US Cross Reference Classification - CCXR (5):

438/127

US-PAT-NO: 6335563

DOCUMENT-IDENTIFIER: US 6335563 B1

TITLE: Semiconductor device, method of fabricating the same, circuit board, and electronic device

DATE-ISSUED: January 1, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hashimoto; Nobuaki	Suwa	N/A	N/A	JP

US-CL-CURRENT: **257/632**, **257/701** , **257/E21.514** , **257/E23.065** , **438/118**

ABSTRACT:

A semiconductor device comprising a flexible substrate having an interconnecting pattern, an anisotropic conductive material arranged on a surface of the flexible substrate on which the interconnecting pattern is provided, a semiconductor chip provided with electrodes connected to the interconnecting pattern through the anisotropic conductive material, and a support member which is applied to the flexible substrate and secures the flatness. The anisotropic conductive material is provided so as to extend outside the semiconductor chip, and the support member is bonded to the flexible substrate via the anisotropic conductive material.

21 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Brief Summary Text - BSTX (34):
(15) In the method of fabricating a semiconductor device, the semiconductor chip may be laid on the adhesive, and **pressure** may be applied to between the semiconductor chip and the flexible substrate to bond the semiconductor chip.

Brief Summary Text - BSTX (35):
(16) In the method of fabricating a semiconductor device, conductive particles may be dispersed in the adhesive, and the conductive particles may electrically connect electrodes of the semiconductor chip to the interconnecting pattern by the **pressure** applied to the adhesive.

Brief Summary Text - BSTX (36):
(17) In the method of fabricating a semiconductor device, the support member may be laid on the adhesive, and **pressure** may be applied to between the support member and the flexible substrate to bond the support member.

Brief Summary Text - BSTX (37):
(18) In the method of fabricating a semiconductor device, the step of applying **pressure** to between the support member and the flexible substrate may

be carried out after the step of applying **pressure** to between the semiconductor chip and the flexible substrate.

Brief Summary Text - BSTX (40):
(20) In the method of fabricating a semiconductor device, the step of applying **pressure** to between the support member and the flexible substrate and the step of applying **pressure** to between the semiconductor chip and the flexible substrate may be carried out at the same time.

Detailed Description Text - DETX (4):
The flexible substrate 10 is formed of a polyimide resin, for example, and has **insulation** characteristics, but the material is not limited to a polyimide resin. In the flexible substrate 10, a plurality of through-holes 12 are formed as shown in FIG. 1. An interconnecting pattern 14 is formed so that it covers the through-holes 12. In areas above the through-holes 12 of the interconnecting pattern 14, there are provided **lands** each having a large area. In this structure, external electrodes 50 (see FIG. 5) can be formed by using the through-holes 12 on the surface of the flexible substrate 10 opposite to the surface with the interconnecting pattern 14 formed thereon. In an area of the interconnecting pattern 14 other than the through-holes 12, **lands** (not shown) for the **connection** to electrodes 32 of a semiconductor chip 30 are formed.

Claims Text - CLTX (29):
wherein the semiconductor chip is laid on the adhesive; and **pressure** is applied between the semiconductor chip and the flexible substrate to bond the semiconductor chip.

Claims Text - CLTX (32):
the conductive particles electrically connect said electrodes of the semiconductor chip to the interconnecting pattern by **pressure** applied to the adhesive.

Claims Text - CLTX (34):
wherein the step of applying **pressure** between the support member and the flexible substrate and the step of applying **pressure** between the semiconductor chip and the flexible substrate are carried out at the same time.

Claims Text - CLTX (37):
pressure is applied between the support member and the flexible substrate to bond the support member.

Claims Text - CLTX (41):
wherein the step of applying **pressure** between the support member and the flexible substrate is carried out after the step of applying **pressure** between the semiconductor chip and the flexible substrate.

Current US Original Classification - CCOR (1):
257/632

Current US Cross Reference Classification - CCXR (1):
257/701

Current US Cross Reference Classification - CCXR (2):
257/E21.514

Current US Cross Reference Classification - CCXR (3):
257/E23.065

Current US Cross Reference Classification - CCXR (4):
438/118

US-PAT-NO: 6365499

DOCUMENT-IDENTIFIER: US 6365499 B1

TITLE: Chip carrier and method of manufacturing and mounting the same

DATE-ISSUED: April 2, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamura; Yoshifumi	Osaka	N/A	N/A	JP
Bessho; Yoshihiro	Osaka	N/A	N/A	JP
Itagaki; Minehiro	Osaka	N/A	N/A	JP

US-CL-CURRENT: **438/613**, **257/E21.511** , **257/E23.067** , **257/E23.069** , 29/840 , 29/841 , **438/108** , **438/118** , **438/126**

ABSTRACT:

In BGA (Ball Grid Array), LGA (**Land** Grid Array) and the like, a resin layer is formed between an external **connecting** electrode of a chip carrier and a circuit wiring board. Consequently, the external **connecting** electrode can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external **connecting** electrode and the circuit wiring board. Thus, the reliability in a thermal shock test can be enhanced. A **connecting** wiring which is conducted to an electrode of a semiconductor device is provided on a surface of an electrical **insulating** board, and the external **connecting** electrode for **connection to a connecting** electrode of the circuit wiring board is provided on a back face of the electrical **insulating** board. The external **connecting** electrode has a solder ball made of a conductor, and the resin layer formed on the side portion thereof.

11 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Abstract Text - ABTX (1):

In BGA (Ball Grid Array), LGA (**Land** Grid Array) and the like, a resin layer is formed between an external **connecting** electrode of a chip carrier and a circuit wiring board. Consequently, the external **connecting** electrode can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external **connecting** electrode and the circuit wiring board. Thus, the reliability in a thermal shock test can be enhanced. A **connecting** wiring which is conducted to an electrode of a semiconductor device is provided on a surface of an electrical **insulating** board, and the external **connecting** electrode for **connection to a connecting** electrode of the circuit wiring board is provided on a back face of the electrical **insulating** board. The external **connecting** electrode has a solder ball made of a conductor, and the resin layer formed on the side portion thereof.

Detailed Description Text - DETX (46):

Then, a hole having a diameter of 0.5 mm is formed on a sheet made of a thermoplastic polyoxyether resin which has a thickness of 0.15 mm by means of a punching machine. The softening point of the resin sheet is 160.degree. C. The external electrode of the chip carrier and the hole portion of the sheet are aligned so as to correspond to each other. The sheet may be temporarily bonded to the chip carrier in the following manner. More specifically, a flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon) is heated to about 160.degree. C. The aligned chip carrier is temporarily bonded to the sheet by means of the heated stainless steel tray. Thus, the sheet can be temporarily bonded to the chip carrier. In addition, the following method can be performed. More specifically, the aligned chip carrier is heated to about 160.degree. C. on the hot plate, and **pressurized** for a desire time by the flat stainless steel tray treated with a polytetrafluoroethylene resin (Teflon). Thus, the sheet made of a resin can be bonded to the chip carrier. While the polyoxyether resin has been used for the sheet in the present example, a resin having a softening point in the range of 160.degree. C. up to a solder paste melting temperature or less also has the same effects. The resin layer should have a softening point of 160.degree. C. or more so as not to be softened by a shelf test at a temperature of 150.degree. C.

Current US Original Classification - CCOR (1):

438/613

Current US Cross Reference Classification - CCXR (1):

257/E21.511

Current US Cross Reference Classification - CCXR (2):

257/E23.067

Current US Cross Reference Classification - CCXR (3):

257/E23.069

Current US Cross Reference Classification - CCXR (6):

438/108

Current US Cross Reference Classification - CCXR (7):

438/118

Current US Cross Reference Classification - CCXR (8):

438/126

US-PAT-NO: 5866441

DOCUMENT-IDENTIFIER: US 5866441 A

TITLE: Inverted chip bonded module with high packaging efficiency

DATE-ISSUED: February 2, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pace; Benedict G.	Ronkonkoma	NY	11779	N/A

US-CL-CURRENT: 438/108, 257/E23.008 , 257/E23.009 , 257/E23.072 , 257/E23.08 , 257/E23.188 , 438/107

ABSTRACT:

An electronic packaging module for inverted bonding of semiconductor devices, integrated circuits, and/or application specific integrated circuits is produced with protuberances on the conductive pattern of the substrate. The protuberances are of a soft, ductile metal capable of being metallurgically bonded to the input/output pads of semiconductor devices. The input/output pads of the semiconductor devices are simultaneously bonded to the protuberances of the packaging module.

20 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Abstract Text - ABTX (1):

An electronic packaging module for inverted bonding of semiconductor devices, integrated circuits, and/or application specific integrated circuits is produced with protuberances on the conductive pattern of the substrate. The protuberances are of a soft, ductile metal capable of being metallurgically bonded to the input/output pads of semiconductor devices. The input/output pads of the semiconductor devices are simultaneously bonded to the protuberances of the packaging module.

Brief Summary Text - BSTX (14):

In another embodiment, the invention is an electronic packaging module or circuit module for semiconductor devices. The base of the module is a planar, insulating substrate. The substrate has a metallic, conductive pattern. The conductive pattern has one or more conductive pattern layers. The conductive pattern layers are formed from either thick or thin film layers, or a combination of thick film layers and thin film layers. The substrate also has metal contacts connected to the conductive pattern, and capable of making electrical connection to another electronic package or a higher level of electronic packaging. The layers of the conductive pattern are separated by insulating layers, and the conductive pattern layers are interconnected by metal filled vias in the insulating layers. The outermost, conductive pattern layer has metal protuberances protruding above the surface of the layer. The

protuberances are made of a soft, ductile metal capable of being metallurgically bonded to the input/output pads of an semiconductor device or **integrated circuit** chip, and are capable of providing input/output connections for semiconductor devices through the connections to the conductive pattern of the package or circuit and through the metal contacts to another electronic package or the next level electronic package.

Brief Summary Text - BSTX (15):

In another embodiment, the invention is a module that employs as a base a ceramic or glass/ceramic **substrate** having a standard pattern of conductive feed-throughs. One side of the base is provided with contact pads, balls or pins connected to the feed-throughs, and the other side of the base is provided with a conductive pattern of one or more conductive pattern layers. Selected feed-throughs required by a custom module design are connected to the conductive pattern and feed-throughs not used in the custom module design are isolated by coating with an insulating layer. The conductive pattern is covered with an insulating layer of a dielectric composition. Laser ablation forms openings in the insulating layer covering the conductive pattern. The openings are made in a pattern corresponding to the input/output pads of one or more semiconductor devices or **integrated circuit** chips. Soft ductile metal is plated into the openings and forms protuberances above the fired layer. The semiconductor devices are metallurgically bonded to the protuberances, making connection through the protuberances to the conductive pattern and through the feed-throughs to the contact pads, balls or pins on the **substrate**.

Brief Summary Text - BSTX (16):

In yet another embodiment, the electronic packaging module is a SCM, single chip module with high packaging efficiency. The high packaging efficiency arises since the SCM may be less than 6 mm (0.15 in.) wider than the bare **integrated circuit** die. The SCM is composed of a planar base with conductive feed-throughs in the base. On one side of the base the conductive feed-throughs are joined to a ball, column, **land,** or pin grid array. On the other side the feed-throughs are **connected** to a conductive pattern of thick and/or thin film metal layers. The conductive pattern layers are separated by **insulating** layers. The topmost, **insulating** layer has metal filled openings in it. The metal in the openings **connects** to underlying conductive pattern layer below, and ends above in soft, ductile metal protuberances protruding above the surface of the **insulating** layer. The protuberances are metallurgically bonded to the input/output pads of a semiconductor device or **integrated circuit** die. The semiconductor device is **connected** through the protuberances and the conductive pattern of the module and the feed-throughs of the **substrate** to a grid array of metal contacts underneath the die, and the area of the **substrate** having the grid array is inside the perimeter of the **integrated circuit** chip.

Detailed Description Text - DETX (11):

In one embodiment the invention, shown in FIG. 1, is a compact, ceramic, chip carrier or SCM, single chip module, 100 with high packaging efficiency. The SCM has a conductive pattern on a ceramic **substrate** 110 as a base. The base has area array contacts 120 for interconnection to second level packaging and a metal or ceramic frame 150 around the semiconductor device or **integrated circuit** chip. The area array of contacts may be an irregular array or a regular array such as a ball, pin, pad or column array. A metal or ceramic plug 170 is brazed to the frame to seal the module.

Detailed Description Text - DETX (47):

A third, dielectric layer is applied over Y-signal, conductive pattern layer. Openings to the Y-signal, conductive pattern layer are made through the dielectric layer. The openings have a diameter at least 10 .mu.m (0.4 mils) and less than 150 .mu.m (6 mils), preferably at least 25 .mu.m (1 mil) and

preferably less than 75 .mu.m (3 mils). The pitch of the openings matches the pitch of the IOs (input/output pads) of the integrated circuits, and the pattern of the openings makes a mirror image of the IO pad pattern of the integrated circuit. The openings are filled with a pure, soft, ductile metal. The metal should be soft enough to permit simultaneously welding of the protuberances to the input/output pads of the integrated circuit die without requiring welding **pressures** so high as to damage the die. Soft, ductile gold is deposited by electroplating or electroless plating. The softness of the gold is dictated by the **pressure** required to thermocompression, thermosonically or ultrasonically bond to the die. If the **pressure** is too great it may damage the die. Large dice with many input/output pads require softer gold to minimize gang bonding **pressure** and reduce the stress on the die. A suitable gold is produced by the Aurall 292 Gold Process, available from LeaRonal Inc., Freeport, N.Y. 11520, USA. The Aurall 292 Gold Process uses a electroplating solution containing 8-16 g/l gold at a pH between 6 and 8, and is believed to contain a phosphonate chelating agent.

Current US Original Classification - CCOR (1):
438/108

Current US Cross Reference Classification - CCXR (1):
257/E23.008

Current US Cross Reference Classification - CCXR (2):
257/E23.009

Current US Cross Reference Classification - CCXR (3):
257/E23.072

Current US Cross Reference Classification - CCXR (4):
257/E23.08

Current US Cross Reference Classification - CCXR (5):
257/E23.188

Current US Cross Reference Classification - CCXR (6):
438/107

US-PAT-NO: **6239496**

DOCUMENT-IDENTIFIER: US 6239496 B1

TITLE: Package having very thin semiconductor chip, multichip module assembled by the package, and method for manufacturing the same

DATE-ISSUED: May 29, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Asada; Junichi	Kawasaki	N/A	N/A	JP

US-CL-CURRENT: 257/777, 257/685 , 257/686 , 257/698 , 257/723 , 257/E21.503 , 257/E23.124 , 257/E25.023

ABSTRACT:

A semiconductor package of this invention has an insulating substrates, wiring layers disposed on the surface of the insulating substrate, a semiconductor chip disposed in a device hole provided in the insulating substrate, inner-joint-conductors for connecting at least part of the bonding pads on the surface of the semiconductor chip to the corresponding inner-joint-conductors and connection lands connected to the wiring layers. The device hole is provided so that it goes through the center of the insulating substrate. The semiconductor chip is thinner than the insulating substrate. Then, this semiconductor chip is disposed in the device hole such that a bottom thereof is flush with a bottom plane of the insulating substrate. Further, this invention provides a MCM in which plural pieces of the thin semiconductor packages are laminated. In the MCM, the semiconductor packages are laminated such that top and bottom faces of the thin silicon chip are inverted. Predetermined connection lands are electrically connected to each other through a connecting conductor. This MCM has a high mechanical strength in its stacked structure and there is a low possibility that crack may occur in the package due to stress in the bending direction.

21 Claims, 26 Drawing figures

Exemplary Claim Number: 17

Number of Drawing Sheets: 15

---------- KWIC ---------

US Patent No. - PN (1):
6239496

US-PAT-NO: 6229209

DOCUMENT-IDENTIFIER: US 6229209 B1

TITLE: Chip carrier

DATE-ISSUED: May 8, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamura; Yoshifumi	Osaka	N/A	N/A	JP
Bessho; Yoshihiro	Osaka	N/A	N/A	JP
Itagaki; Minehiro	Osaka	N/A	N/A	JP

US-CL-CURRENT: 257/737, 257/700 , 257/778 , 257/E21.511 , 257/E23.067 , 257/E23.069

ABSTRACT:

In BGA (Ball Grid Array), LGA (Land Grid Array) and the like, a resin layer is formed between an external connecting electrode of a chip carrier and a circuit wiring board. Consequently, the external connecting electrode can be prevented from cracking due to a difference between the coefficients of thermal expansion of the external connecting electrode and the circuit wiring board. Thus, the reliability in a thermal shock test can be enhanced. A connecting wiring which is conducted to an electrode of a semiconductor device is provided on a surface of an electrical insulating board, and the external connecting electrode for connection to a connecting electrode of the circuit wiring board is provided on a back face of the electrical insulating board. The external connecting electrode has a solder ball made of a conductor, and the resin layer formed on the side portion thereof.

35 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

US Patent No. - PN (1):
6229209

US-PAT-NO: 5624268

DOCUMENT-IDENTIFIER: US 5624268 A

TITLE: Electrical connectors using anisotropic conductive films

DATE-ISSUED: April 29, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maeda; Ryu	Urawa	N/A	N/A	JP
Tateishi; Akira	Hachioji	N/A	N/A	JP
Tazai; Shunsuke	Fuchu	N/A	N/A	JP

US-CL-CURRENT: 439/66, 257/E23.067 , 439/91

ABSTRACT:

This invention presents a new anisotropic conductive film for conductive connections, its method of manufacture, and connectors which use the same, which reduces the connection resistance of semiconductor and similar devices, to the circuit substrates, and simultaneously simplifies the repair. Copper foil 2 is bonded on both sides to an electrical insulating film 3. Holes are formed in the copper foil 2 by etching, and through-holes 5 are formed in the aforesaid electrical insulating film 3, using copper foil 2 as a mask for etching. Next, the through-holes 5 are filled with a conductive elastomer 6, and hardened. The copper foil 2 is then etched to form protuberances 4 of elastomer 6 having the same viscosity. The conducting elastomer 6 protuberance 4 on one side makes contact with the semiconductor device pad, while the protuberance 4 on the other side makes contact with the substrate-side pad. A conductive connection is made by pressing both together.

4 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

This invention presents a new anisotropic conductive film for conductive connections, its method of manufacture, and connectors which use the same, which reduces the connection resistance of semiconductor and similar devices, to the circuit substrates, and simultaneously simplifies the repair. Copper foil 2 is bonded on both sides to an electrical insulating film 3. Holes are formed in the copper foil 2 by etching, and through-holes 5 are formed in the aforesaid electrical insulating film 3, using copper foil 2 as a mask for etching. Next, the through-holes 5 are filled with a conductive elastomer 6, and hardened. The copper foil 2 is then etched to form protuberances 4 of elastomer 6 having the same viscosity. The conducting elastomer 6 protuberance 4 on one side makes contact with the semiconductor device pad, while the protuberance 4 on the other side makes contact with the substrate-side pad. A conductive connection is made by pressing both together.

TITLE - TI (1):

conductive particles

Electrical connectors using anisotropic conductive films

US-PAT-NO: 6002180

DOCUMENT-IDENTIFIER: US 6002180 A

TITLE: Multi chip module with conductive adhesive layer

DATE-ISSUED: December 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Akram; Salman	Boise	ID	N/A	N/A
Wood; Alan G.	Boise	ID	N/A	N/A
Farnworth; Warren M.	Nampa	ID	N/A	N/A

US-CL-CURRENT: 257/783, 257/782 , 257/E21.503 , 257/E21.511 , 257/E21.514 , 257/E23.004

ABSTRACT:

A method for forming a chip module such as a multi chip module or a memory module is provided. The multi chip module includes a substrate configured to mount a plurality of semiconductor dice thereon. The substrate includes raised contact members formed in patterns that correspond to the locations of bond pads on the dice. An **anisotropic conductive** adhesive layer is formed between the contact members on the substrate and the bond pads on the dice to secure the dice to the substrate and form an electrical connection therebetween. In addition, an underfill layer can be formed between the dice and substrate to fill the gap therebetween and further secure the dice to the substrate. Conductors and input/output pads formed on the substrate form electrical paths to and from the contact members. To form a memory module, one or more multi chip modules can be mounted to a supporting substrate having an edge **connector** in electrical communication with the conductors and with contact members on the substrates.

26 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for forming a chip module such as a multi chip module or a memory module is provided. The multi chip module includes a substrate configured to mount a plurality of semiconductor dice thereon. The substrate includes raised contact members formed in patterns that correspond to the locations of bond pads on the dice. An **anisotropic conductive** adhesive layer is formed between the contact members on the substrate and the bond pads on the dice to secure the dice to the substrate and form an electrical connection therebetween. In addition, an underfill layer can be formed between the dice and substrate to fill the gap therebetween and further secure the dice to the substrate. Conductors and input/output pads formed on the substrate form electrical paths to and from the contact members. To form a memory module, one or more multi chip modules can be mounted to a supporting substrate having an edge **connector** in electrical communication with the conductors and with contact members on the substrates.

US-PAT-NO: 5789278

DOCUMENT-IDENTIFIER: US 5789278 A

TITLE: Method for fabricating chip modules

DATE-ISSUED: August 4, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Akram; Salman	Boise	ID	N/A	N/A
Wood; Alan G.	Boise	ID	N/A	N/A
Farnworth; Warren M.	Nampa	ID	N/A	N/A

US-CL-CURRENT: 438/118, 257/E21.503 , 257/E21.511 , 257/E21.514 , 257/E23.004 , 438/114

ABSTRACT:

A method for forming a chip module such as a multi chip module or a memory module is provided. The multi chip module includes a substrate configured to mount a plurality of semiconductor dice thereon. The substrate includes raised contact members formed in patterns that correspond to the locations of bond pads on the dice. An anisotropic conductive adhesive layer is formed between the contact members on the substrate and the bond pads on the dice to secure the dice to the substrate and form an electrical connection therebetween. In addition, an underfill layer can be formed between the dice and substrate to fill the gap therebetween and further secure the dice to the substrate. Conductors and input/output pads formed on the substrate form electrical paths to and from the contact members. To form a memory module, one or more multi chip modules can be mounted to a supporting substrate having an edge connector in electrical communication with the conductors and with contact members on the substrates.

31 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for forming a chip module such as a multi chip module or a memory module is provided. The multi chip module includes a substrate configured to mount a plurality of semiconductor dice thereon. The substrate includes raised contact members formed in patterns that correspond to the locations of bond pads on the dice. An anisotropic conductive adhesive layer is formed between the contact members on the substrate and the bond pads on the dice to secure the dice to the substrate and form an electrical connection therebetween. In addition, an underfill layer can be formed between the dice and substrate to fill the gap therebetween and further secure the dice to the substrate. Conductors and input/output pads formed on the substrate form electrical paths to and from the contact members. To form a memory module, one or more multi chip modules can be mounted to a supporting substrate having an edge connector in electrical communication with the conductors and with contact members on the substrates.

US-PAT-NO: 5624268

DOCUMENT-IDENTIFIER: US 5624268 A

TITLE: Electrical connectors using anisotropic conductive films

DATE-ISSUED: April 29, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maeda; Ryu	Urawa	N/A	N/A	JP
Tateishi; Akira	Hachioji	N/A	N/A	JP
Tazai; Shunsuke	Fuchu	N/A	N/A	JP

US-CL-CURRENT: 439/66, 257/E23.067 , 439/91

ABSTRACT:

This invention presents a new anisotropic conductive film for conductive connections, its method of manufacture, and connectors which use the same, which reduces the connection resistance of semiconductor and similar devices, to the circuit substrates, and simultaneously simplifies the repair. Copper foil 2 is bonded on both sides to an electrical insulating film 3. Holes are formed in the copper foil 2 by etching, and through-holes 5 are formed in the aforesaid electrical insulating film 3, using copper foil 2 as a mask for etching. Next, the through-holes 5 are filled with a conductive elastomer 6, and hardened. The copper foil 2 is then etched to form protuberances 4 of elastomer 6 having the same viscosity. The conducting elastomer 6 protuberance 4 on one side makes contact with the semiconductor device pad, while the protuberance 4 on the other side makes contact with the substrate-side pad. A conductive connection is made by pressing both together.

4 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

This invention presents a new anisotropic conductive film for conductive connections, its method of manufacture, and connectors which use the same, which reduces the connection resistance of semiconductor and similar devices, to the circuit substrates, and simultaneously simplifies the repair. Copper foil 2 is bonded on both sides to an electrical insulating film 3. Holes are formed in the copper foil 2 by etching, and through-holes 5 are formed in the aforesaid electrical insulating film 3, using copper foil 2 as a mask for etching. Next, the through-holes 5 are filled with a conductive elastomer 6, and hardened. The copper foil 2 is then etched to form protuberances 4 of elastomer 6 having the same viscosity. The conducting elastomer 6 protuberance 4 on one side makes contact with the semiconductor device pad, while the protuberance 4 on the other side makes contact with the substrate-side pad. A conductive connection is made by pressing both together.

TITLE - TI (1):

Electrical connectors using anisotropic conductive films

PAT-NO: JP411329541A

DOCUMENT-IDENTIFIER: JP 11329541 A

TITLE: ANISOTROPIC CONDUCTIVE CONNECTOR

PUBN-DATE: November 30, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
ITO, SHIGENORI	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
JAPAN AVIATION ELECTRONICS IND LTD	N/A

APPL-NO: JP10146607

APPL-DATE: May 12, 1998

INT-CL (IPC): H01R011/01

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a low-resistant connector usable as a connector for LSI by holding a layered product between a pair of dielectric boards having conductive portions contactable with a conductive layer.

SOLUTION: An anisotropic conductive rubber connector 10 is held on its both sides between a pair of dielectric boards 20 constituted with a band-shaped insulating portion 22 and conductive portions 21 provided in a constant interval on the surface of the insulating portion 22. During un-pressurization the height of the dielectric boards 20 is lower than that of the anisotropic conductive rubber connector 10, and when an LSI 40 is pressurized balls 41 of the LSI 40 abut to electrodes 51 of a printed board 50 through the anisotropic conductive rubber connector 10. Then, the anisotropic conductive rubber connector 10 is pressed to deform and to be pressed onto the conductive portions 21, and contact stability of conductive rubber of the anisotropic conductive rubber connector 10 with the conductive portions 21 is improved. Therefore, current flows through the conductive rubber of the anisotropic conductive rubber connector 10, and through the conductive portions 21 of the dielectric boards 20.

PAT-NO: JP411074051A

DOCUMENT-IDENTIFIER: JP 11074051 A

TITLE: CONNECTING STRUCTURE OF ELECTRIC COMPONENT IN COMMUNICATION TERMINAL EQUIPMENT

PUBN-DATE: March 16, 1999

INVENTOR-INFORMATION:
NAME
HASEGAWA, MASAYUKI
AOKI, YOSHINORI
HOSHIJIMA, TOSHIYUKI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SANYO ELECTRIC CO LTD	N/A

APPL-NO: JP09234590

APPL-DATE: August 29, 1997

INT-CL (IPC): H01R023/68, H04B001/38 , H04M001/02 , H04M001/23

ABSTRACT:

PROBLEM TO BE SOLVED: To miniaturize a circuit board, by superposing an electrode group of a key sheet on an electrode group of a circuit board each other, and sandwiching the superposed part by pressure between a part of a frame body and the circuit board, and electrically connecting the corresponding electrodes.

SOLUTION: An electrode group 51 of a key sheet 5 is superposed on an electrode group 62 of a circuit board 6 through an **anisotropic conductive** sheet 60, and in this state, a frame body 3 mounted with a reinforcing member 4 is engaged with the circuit board 6 and the key sheet 5. Thus, an end part of the key sheet 5 and the circuit board 6 are sandwiched between a lower pressure part 34 of the frame body 3 and a hook 31, therefore, the **anisotropic conductive** sheet 60 and both the electrode groups 62, 51 are pinched from above and beneath. In the connecting structure of the key sheet 5 like this, the simple connecting structure that the electrode group 51 of the key sheet 5 and the electrode group 62 of the circuit board 6 are only superposed and pinched is used, therefor, a **connector** is unnecessary, thus, the connecting structure can be arranged in the small space.

PAT-NO: JP410125372A

DOCUMENT-IDENTIFIER: JP 10125372 A

TITLE: ANISOTROPIC CONDUCTIVE CONNECTOR AND MANUFACTURE THEREOF

PUBN-DATE: May 15, 1998

INVENTOR-INFORMATION:
NAME
TATSUKI, MASAHIKO
TANAKA, MASAYOSHI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOKAI RUBBER IND LTD	N/A

APPL-NO: JP08276116

APPL-DATE: October 18, 1996

INT-CL (IPC): H01R011/01, H01B005/16 , H01R043/00

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an **anisotropic conductive connector** capable of preventing a conductive material from falling by applying the constitution that a conductive bump with a top part projected toward both of the upper and lower sides of a sheet-type fiber substrate having fiber intersections, so as to keep the bump in such a state as containing the fiber intersections.

SOLUTION: A plurality of bumps 4 (bumps made of various metals such as gold, silver and copper, or bumps made of the alloys thereof) are arranged on a woven fabric 1 having the intersections 3 where fibers 2 are arranged horizontally and vertically, so that the adjacent bumps 4 maintain a constant interval from each other, and the top parts 4a of the bumps 4 project to both of the upper and lower sides of the fabric 1. Also, the conductive bumps 4 are kept in such a state as to contain the fiber intersections 3. As a result, conductivity appears only along the thickness of the woven fabric 1 and the part of the fabric 1 along a direction (bilateral direction) intersecting a thickness-wise direction is electrically insulated, thereby allowing inexpensive and mass production of an **anisotropic conductive connector** having high conductive connection reliability.

PAT-NO: JP410125372A

DOCUMENT-IDENTIFIER: JP 10125372 A

TITLE: ANISOTROPIC CONDUCTIVE CONNECTOR AND MANUFACTURE THEREOF

PUBN-DATE: May 15, 1998

INVENTOR-INFORMATION:
NAME
TATSUKI, MASAHIKO
TANAKA, MASAYOSHI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOKAI RUBBER IND LTD	N/A

APPL-NO: JP08276116

APPL-DATE: October 18, 1996

INT-CL (IPC): H01R011/01, H01B005/16 , H01R043/00

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an anisotropic conductive connector capable of preventing a conductive material from falling by applying the constitution that a conductive bump with a top part projected toward both of the upper and lower sides of a sheet-type fiber substrate having fiber intersections, so as to keep the bump in such a state as containing the fiber intersections.

SOLUTION: A plurality of bumps 4 (bumps made of various metals such as gold, silver and copper, or bumps made of the alloys thereof) are arranged on a woven fabric 1 having the intersections 3 where fibers 2 are arranged horizontally and vertically, so that the adjacent bumps 4 maintain a constant interval from each other, and the top parts 4a of the bumps 4 project to both of the upper and lower sides of the fabric 1. Also, the conductive bumps 4 are kept in such a state as to contain the fiber intersections 3. As a result, conductivity appears only along the thickness of the woven fabric 1 and the part of the fabric 1 along a direction (bilateral direction) intersecting a thickness-wise direction is electrically insulated, thereby allowing inexpensive and mass production of an anisotropic conductive connector having high conductive connection reliability.

PAT-NO: JP409180792A

DOCUMENT-IDENTIFIER: JP 09180792 A

TITLE: HEAT SEAL CONNECTOR

PUBN-DATE: July 11, 1997

INVENTOR-INFORMATION:
NAME
FUJINAMI, NAOKI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SHIN ETSU POLYMER CO LTD	N/A

APPL-NO: JP07340245

APPL-DATE: December 27, 1995

INT-CL (IPC): H01R011/01, H01R009/09 , H05K003/36

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a heat seal connector having a high bending resistance and electrical insulation, and allowing manufacturing at low cost.

SOLUTION: A heat seal connector 1 has a coated layer formed out of an anisotropic conductive adhesive 6 on the entire surface of an insulating flexible substrate 3 having the prescribed circuit pattern 2 of a conductive component, including the area of the circuit pattern 2. Also, an ink overlay 7 formed to thickness between 5μm and 30μm, and made of the coated layer of a resist ink containing a foaming agent is formed on the coated layer of the adhesive 6 except for the connecting terminal part of the circuit pattern 2 thereon.

PAT-NO: JP408327704A

DOCUMENT-IDENTIFIER: JP 08327704 A

TITLE: ADAPTER DEVICE FOR INSPECTING CIRCUIT BOARD

PUBN-DATE: December 13, 1996

INVENTOR-INFORMATION:
NAME
HANAWA, KAZUMI
SUZUKI, KAZUO
KOYAMA, KENICHI
IGARASHI, HISAO

ASSIGNEE-INFORMATION:

NAME	COUNTRY
JAPAN SYNTHETIC RUBBER CO LTD	N/A

APPL-NO: JP07334720

APPL-DATE: December 22, 1995

INT-CL (IPC): G01R031/28, H01R011/01

ABSTRACT:

PURPOSE: To provide the adapter device for inspecting a circuit board, which can be manufactured advantageously at a low cost, wherein the required electric connections can be securely achieved even when the pitch of the electrodes under inspection in a circuit board is minute and the electrodes have the high density and the complicated structure, the excellent electric connecting state is stably maintained for environment change and connecting reliability is high.

CONSTITUTION: An adapter device 10 comprises an adapter main body 12, which has a lattice-shaped terminal electrodes 30 at the lower surface and connecting electrodes 40 corresponding to electrodes under inspection at the upper surface, and an anisotropic conductive connector layer 15, which is provided on the upper surface of the adapter main body 12 as a unitary body. Furthermore, an insulating layer 18 of the adapter main body 12 is constituted of thermosetting resin sheets 23 and 25 provided on the surface to be attached by thermocompressing bonding. Or a conducting-path forming part 17 on the insulating layer 18 is formed of a metallic foil provided on the insulating layer 18 by thermocompression bonding.

PAT-NO: JP406231818A

DOCUMENT-IDENTIFIER: JP 06231818 A

TITLE: ANISOTROPIC CONDUCTIVE CONNECTOR WITH ELASTICITY

PUBN-DATE: August 19, 1994

INVENTOR-INFORMATION:
NAME
KANETO, MASAYUKI
MORITA, NAOHARU
BABA, TOSHIKAZU
NAITO, TOSHIKI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NITTO DENKO CORP	N/A

APPL-NO: JP05014589

APPL-DATE: February 1, 1993

INT-CL (IPC): H01R011/01

US-CL-CURRENT: 439/86, 439/474

ABSTRACT:

PURPOSE: To provide an anisotropic conductive connector, having a good cushoin property without coming-off of a connected part due to stress relaxation, even when outside stress or repetitive stress is applied after connection.

CONSTITUTION: An insulating film 1 is used, in which elastic body layers 11 having an impact resilience of 5-70 % are laminated on one side surface or both surfaces. A conductive path 2, filled with metallic substance, is formed in the thickness direction of the film 1. The conductive path 2 reaches the front and rear surfaces of the insulating film 1, and metallic bumps 3 are formed on a conductive path end.